II. REMARKS

Claims 1-14 and 28-29 are pending. Claims 15-27 were previously cancelled (in response to restriction requirement), and claims 28-29 have been newly added. Attached hereto is Appendix A showing the change made to the specification. Reconsideration is respectfully requested.

1. Specification

The Examiner noted that reference number 54 was inadvertently used to represent both the control gate and the floating gate in the paragraph on page 7, lines 14-25. This paragraph has been amended to correct this informality.

2. Rejection of Claims 1-2 and 4-8 Under § 102(e)

Claims 1-2 and 4-8 were rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 6,420,753 (Hoang). The Applicants respectfully traverse this rejection.

Claim 1 recites a memory cell and an MOS transistor formed in the memory area and the peripheral area of the substrate, respectively. The memory cell includes a floating gate and a control gate, and the MOS transistor includes a poly gate. A continuously formed insulating layer of material has a first portion disposed between the control gate and the floating gate, and a second portion disposed between the poly gate and the substrate. The first portion has a thickness permitting Folwer-Nordheim tunneling, and the second portion has a thickness greater than that of the first portion. While Hoang utilizes a deposited insulation layer 206 that extends between the floating and control gates, as well as between the poly gate and the substrate, this insulation layer 206 is not formed with a varying thickness as recited by claim 1. Thus, it is respectfully submitted that claim 1 is not anticipated Hoang.

The Examiner states on page 4 of the office action that, as shown in Huang Fig. 6, the portion of layer 206 disposed between the control gate 210 and the floating gate 204 meets the first portion of the claimed insulating layer, and insulating layers 206/202 disposed between poly gate 208 and substrate 200 meet the second portion of the claimed insulating layer. The Applicants respectfully traverse this conclusion for several reasons. First, claim 1 is directed to a

continuous layer of material, having portions of different thicknesses. Thus, insulation layer 202 in combination with insulation layer 206 cannot be relied upon to meet the elements of claim 1. Second, claim 1 recites that the insulation layer extends between the floating gate and the control gate in the memory cell area, which layer 202 does not. Thus, it is respectfully submitted that Hoang does not anticipate claim 1.

Claims 2 and 4-8 all depend on claim 1, and are therefore deemed allowable for the reasons set forth above. Further, Hoang fails to teach elements recited in these dependent claims. For example, claim 7 recites the insulation layer second portion is formed directly on the peripheral area of the substrate, and the poly gate is formed directly on the insulating layer second portion. While the poly gate 208 in Hoang is apparently formed directly on insulating layer 206, insulating layer 206 is formed directly on layer 102, not directly on the peripheral area of the substrate as recited in claim 7.

It is therefore respectfully submitted that claims 1-2 and 4-8 are not anticipated by Hoang, and that this rejection should be withdrawn.

3. Rejection of Claims 3 and 9-14 Under § 103(a)

Claims 3 and 9-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,429,073 (Furuhata). It is believed the Examiner meant to state that these claims are rejected over Furuhata in combination with Hoang, because the Examiner makes numerous references to Hoang and to the reasons for rejecting claim 1. Furuhata is apparently cited merely for teaching a second source and a second drain in a memory device. Therefore, the Applicants assume as such, and respectfully traverse this rejection on that basis.

Claim 3 is dependent upon claim 1, and is therefore deemed allowable for the reasons set forth above in Part 2. The addition of Furuhata fails to cure the deficiencies of Hoang.

Claim 9 is similar to claim 1, in that it recites a continuously formed insulating layer having a first portion disposed between the control gate and the floating gate, and a second portion disposed between the poly gate and the substrate, where the first portion has a thickness permitting Folwer-Nordheim tunneling and the second portion has a thickness greater than the first portion. As stated above in Part 2, Hoang fails to teach a continuous layer of insulating

material having a greater thickness in the peripheral region than in the memory region as recited in claim 9. Furuhata clearly fails to cure this deficiency. Thus, it is submitted that claim 9 is not rendered obvious over Hoang and/or Furuhata.

Claims 10-14 all depend on claim 9, and are therefore deemed allowable for the reasons set forth above. Further, Hoang and Furuhata fail to teach elements recited in these dependent claims. For example, as stated above with respect to claim 7, Hoang fails to teach the insulation layer second portion being formed directly on the peripheral area of the substrate, and the poly gate being formed directly on the insulating layer second portion. Instead, poly gate 208 of Hoang is apparently formed directly on insulating layer 206, and insulating layer 206 is formed directly on insulating layer 202.

It is therefore respectfully submitted that claims 3, and 9-14 are not rendered obvious by Hoang and/or Furuhata, and that this rejection should be withdrawn.

4. New claims

Claims 28 and 29 have been newly added. These claims each recite the combination of the insulating layer first portion formed directly against the floating gate, the control gate formed directly on the insulating layer first portion, the insulating layer second portion formed directly on the peripheral area of the substrate, and the poly gate formed directly on the insulating layer second portion. It is respectfully submitted that neither Hoang or Furuhata teach or suggest such a memory device.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

Respectfully submitted,

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By: _____

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APPENDIX A: MARKINGS TO SHOW CHANGES MADE

Paragraph on page 7, lines 14-25:

In the memory cell area 32, a channel region 66 is defined in the substrate between the source 58 and drain 60. Poly layer 38 forms the cell's floating gate, which is disposed over and insulated from a first portion of the channel region 66 and a portion of the source region 58. Poly block 54 forms the cell's control gate, which includes a first portion 54a that is disposed over and insulated from a second portion of the channel region 66 and a portion of the drain 60, and is laterally adjacent to and insulated from the floating gate 38. The control gate 54 has a second portion 54b that is disposed over (vertically adjacent to) and insulated from the floating gate [54] 38. A notch 68 is formed in the control gate 54 by the nitride spacer 52, which helps prevent reverse tunneling back to the floating gate or to the substrate. The non-volatile memory cell is of the split gate type as described in U.S. Patent No. 5,572,054, which discloses the operation of such a non-volatile memory cell and an array formed thereby, and is hereby incorporated herein by reference.